Optimizing Hardware/Software Development for ARM based Embedded Designs

arm

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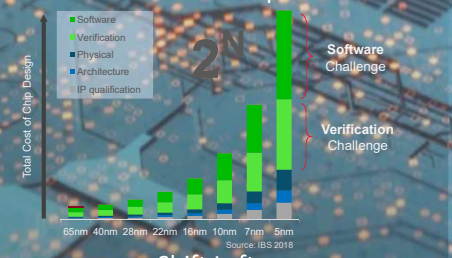
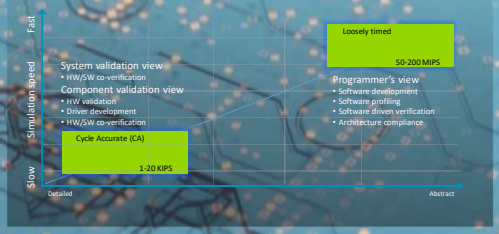
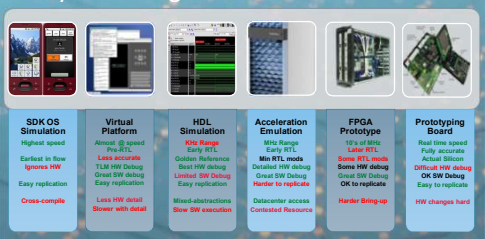
Software Drives Development Cost!



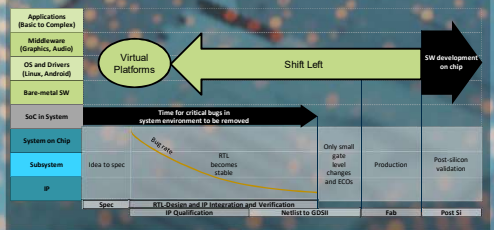
System on Chip Simulation Views



Dynamic Engines – No "One Fits All"

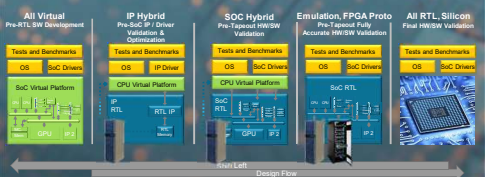


Shift Left



Development Tools for All Arm Cores

Mixed Level Abstractions



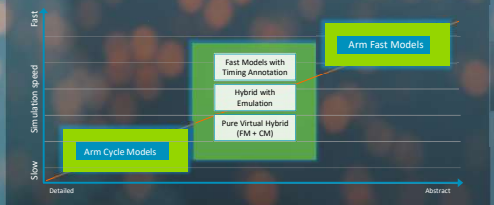
Addressing the Model Landscape

Compiled directly from RTL

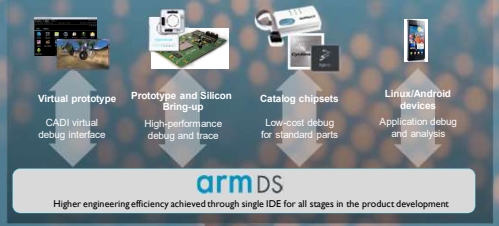
- Retain 100% of functionality
- Cycle Model Studio for customer RTL
- Arm providing Cycle Models of most Arm IP
- Visibility options to enable system debug by hardware or software designers

Fast, functionally complete models

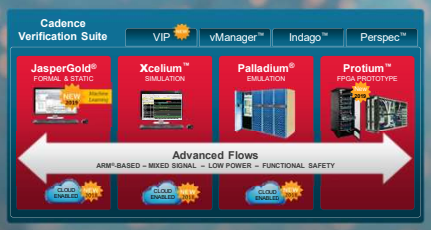
- 10s to 100s of MIPS speed for OS boots and SW development
- Accuracy to run even the lowest level unmodified binaries
- Timing annotation for system optimization
- Earliest availability models
- Architecture models represent ISA
- Developed in conjunction with RTL



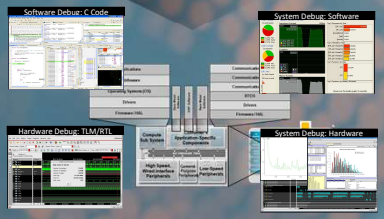
Support for All Stages of Development



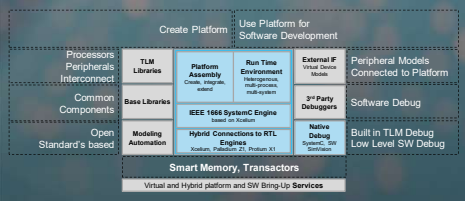
Verification Options



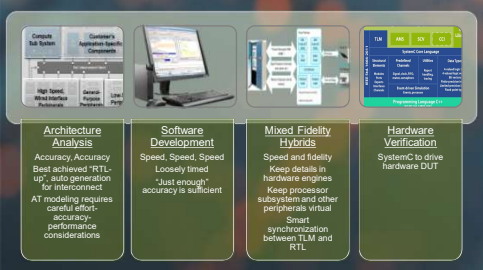
Hardware/Software Debug



Virtual Platform Environment



Related Other Use Models

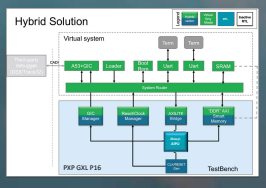


Palladium - Fast Models Hybrid Use Case

Arm China adopts Palladium™ Hybrid solution in latest generation of AIPU development

Platform:

- Palladium
- Arm Fast models
- Arm DS-5 debugger



Benefit:

- Build up complete SoC HW/SW validation environment in days
- Run software bring up and validation with high performance (1000x)

Related User Examples